

The diagram illustrates a multi-channel signal processing system, likely for a multi-channel video signal, organized into three main functional blocks: N1, N2, and N3.

- Block N1 (Left):** This block contains a differential amplifier stage. It includes a differential pair of transistors Q1 and Q2, with a tail resistor R12 connected to ground. The gates of Q1 and Q2 are driven by a common-mode signal from a voltage divider (R7, R8) connected to Vcc. The drains of Q1 and Q2 are connected to a load resistor R9 and a coupling capacitor C4, respectively. The output of this stage is fed into the input of Block N2.
- Block N2 (Middle):** This block serves as a signal distribution and conditioning stage. It features a differential pair of transistors Q3 and Q4, with a tail resistor R10. The gates of Q3 and Q4 are driven by a common-mode signal from a voltage divider (R11, R12) connected to Vcc. The drains of Q3 and Q4 are connected to a load resistor R11 and a coupling capacitor C6, respectively. The output of this stage is fed into the input of Block N3.
- Block N3 (Right):** This block contains a differential amplifier stage. It includes a differential pair of transistors Q5 and Q6, with a tail resistor R12 connected to ground. The gates of Q5 and Q6 are driven by a common-mode signal from a voltage divider (R11, R12) connected to Vcc. The drains of Q5 and Q6 are connected to a load resistor R11 and a coupling capacitor C6, respectively. The output of this stage is fed into the input of Block N4.

The system is powered by a Vcc supply and a ground connection. The output of the final stage (N4) is connected to a load resistor R12. The diagram also shows various other components such as resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12), capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10), and diodes (D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12).

FIG. 2A

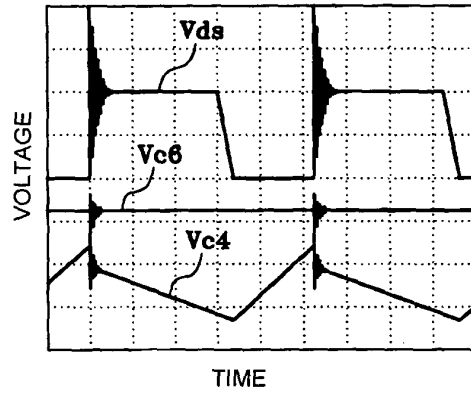


FIG. 2B

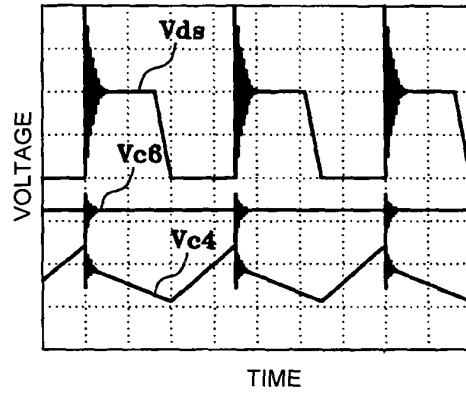


FIG. 2C

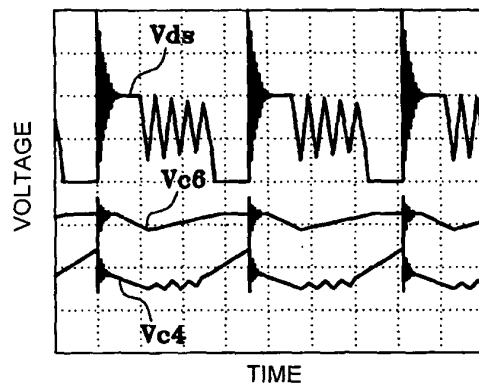


FIG. 2D

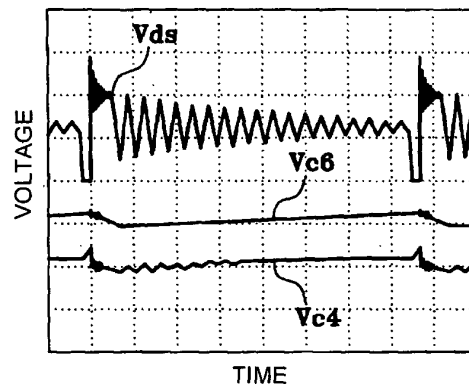


FIG. 3

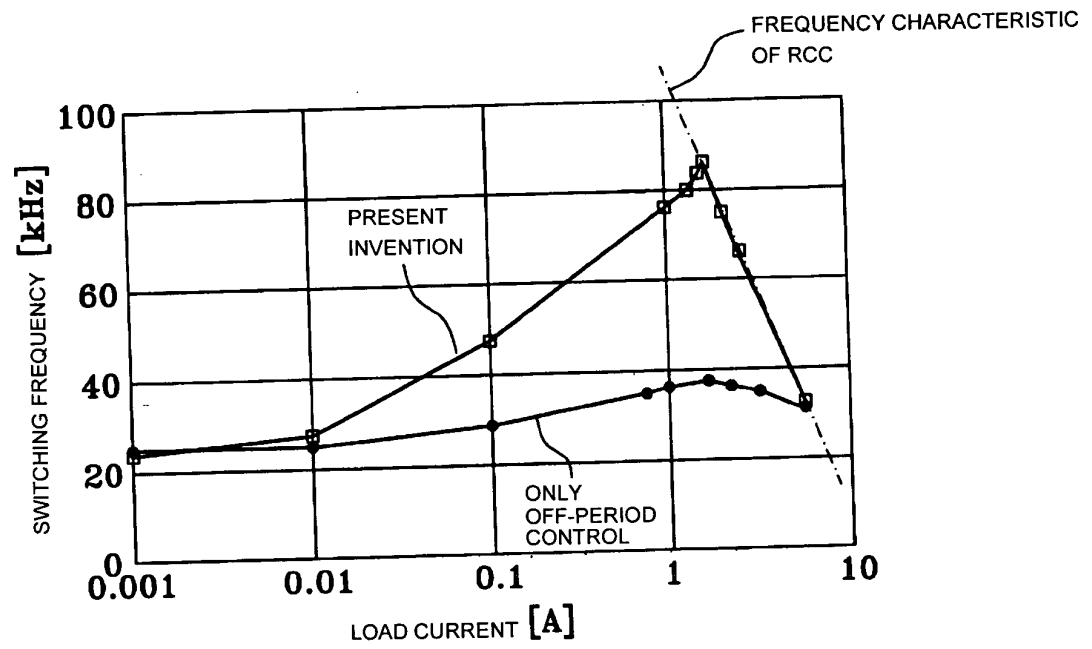


FIG. 4

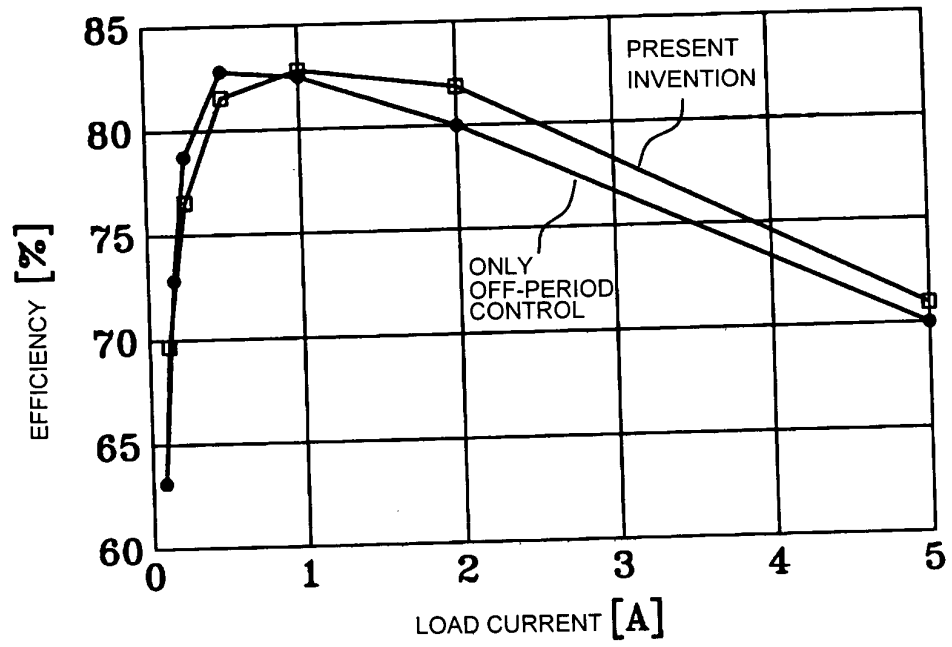


FIG. 5

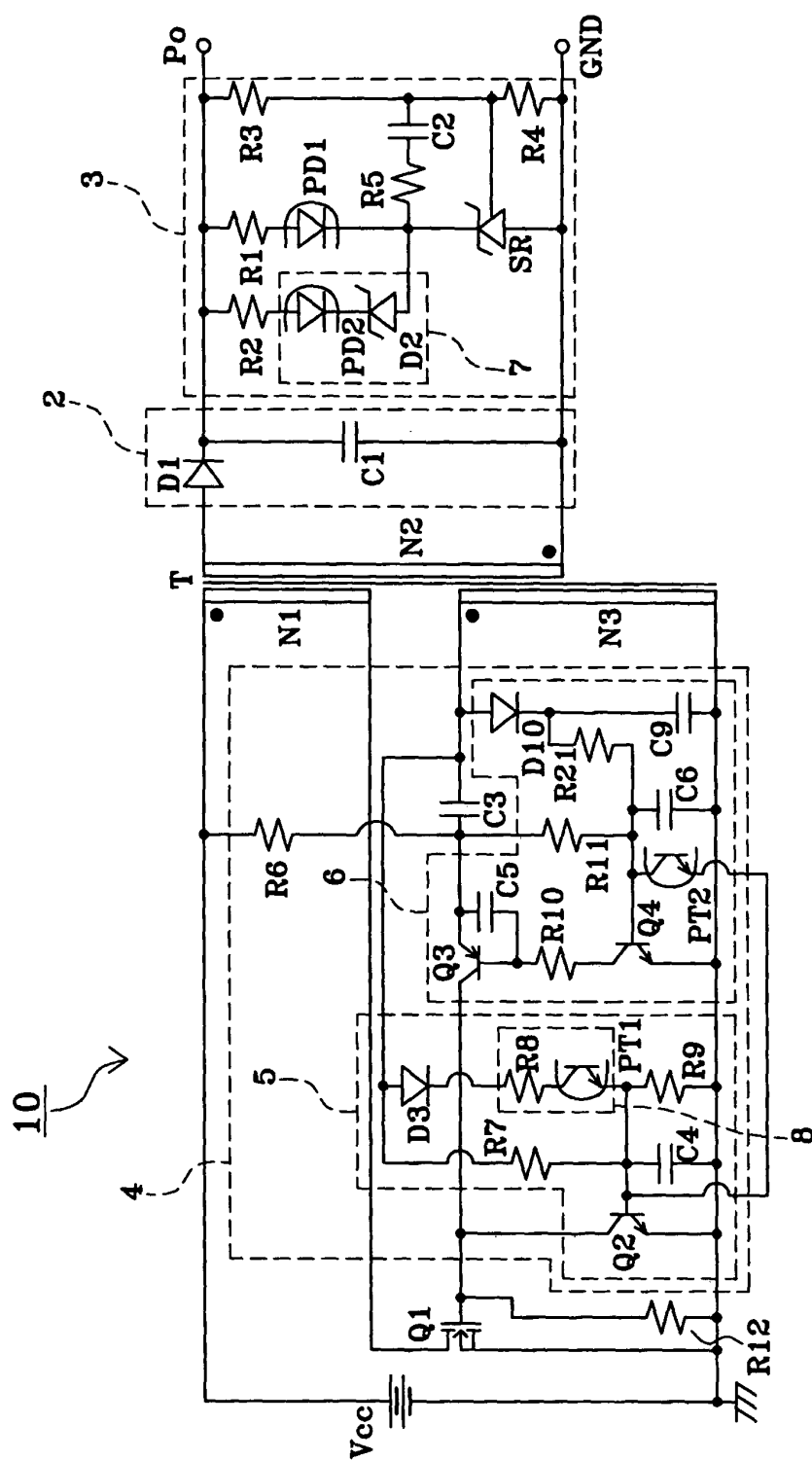


FIG. 6

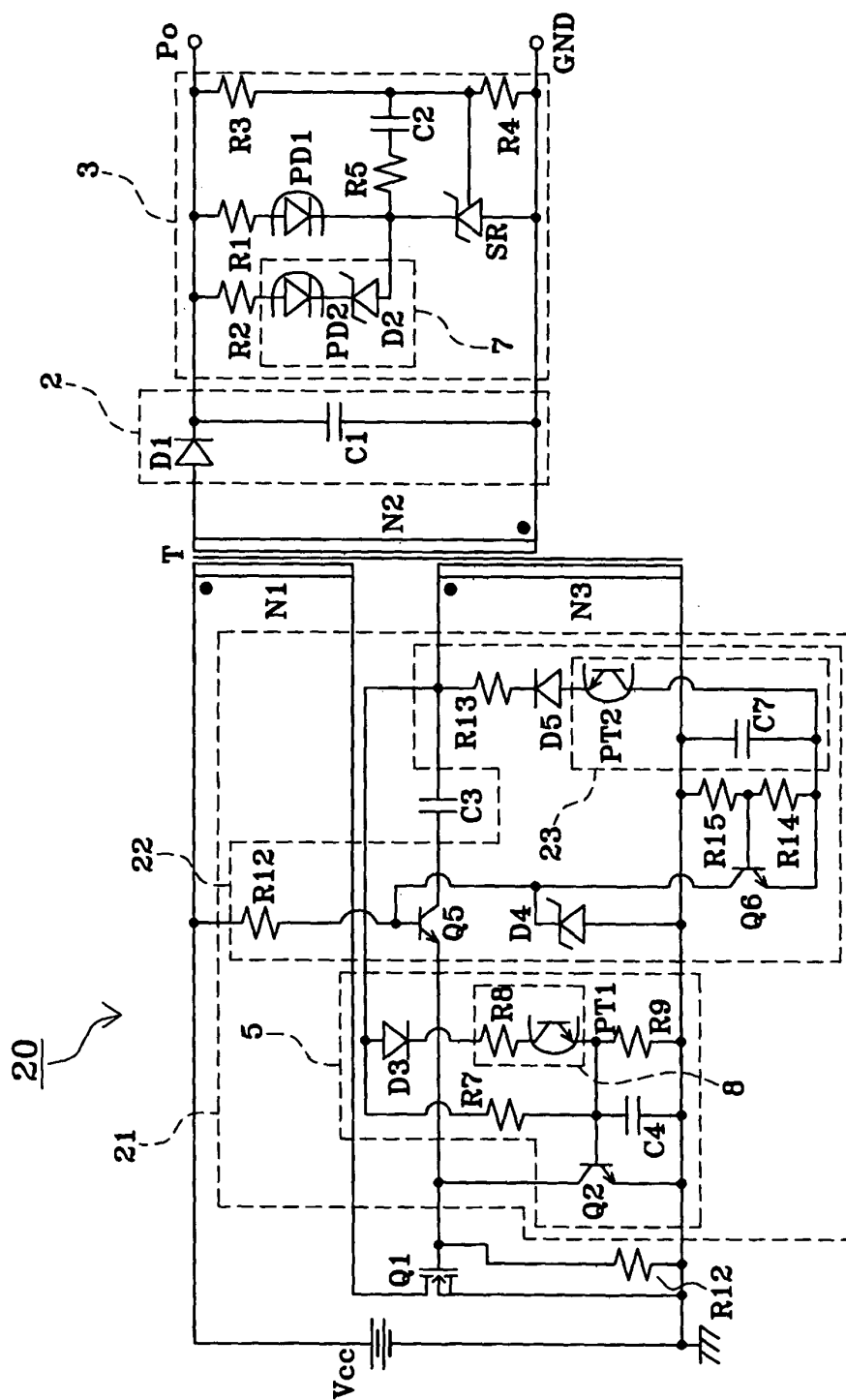


FIG. 7

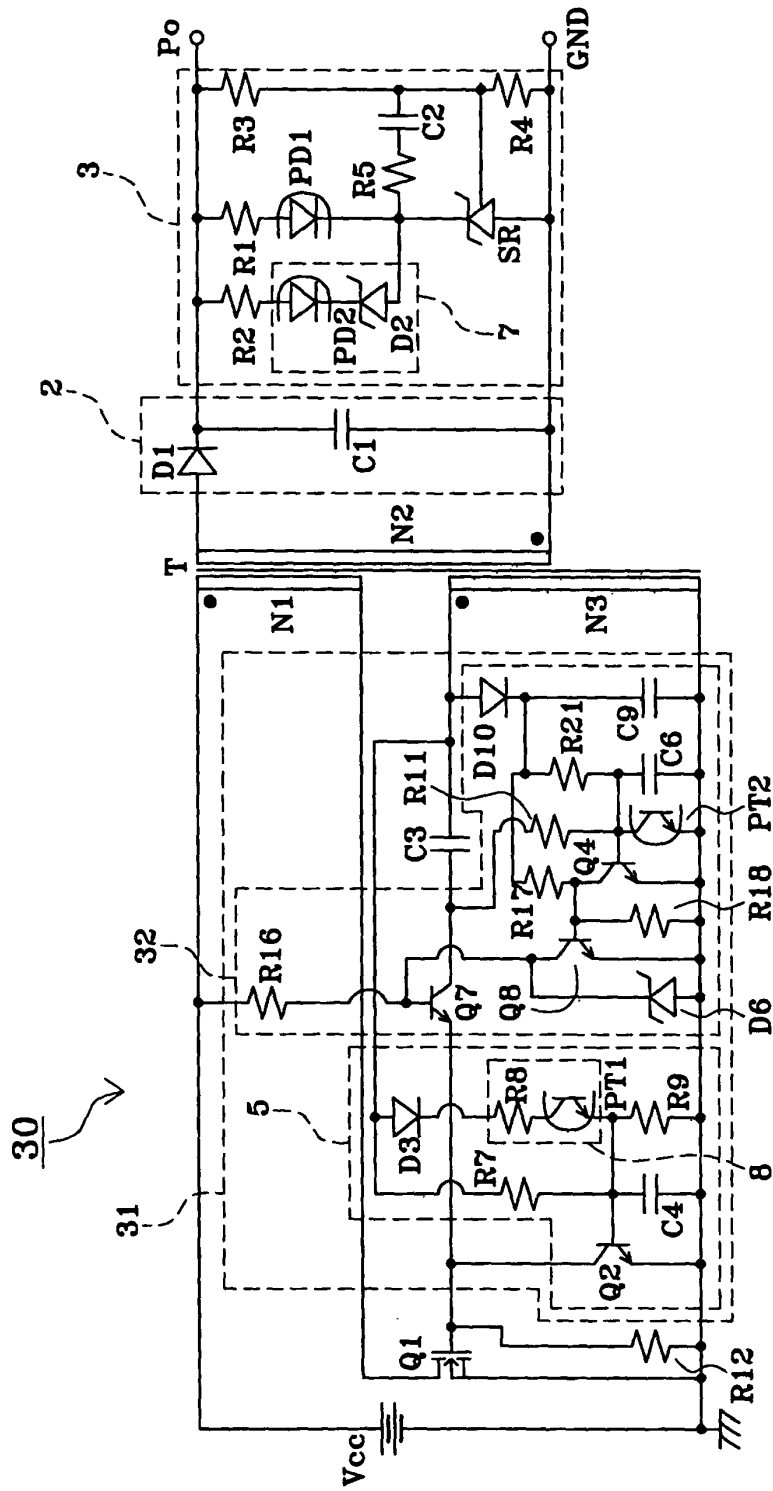


FIG. 8

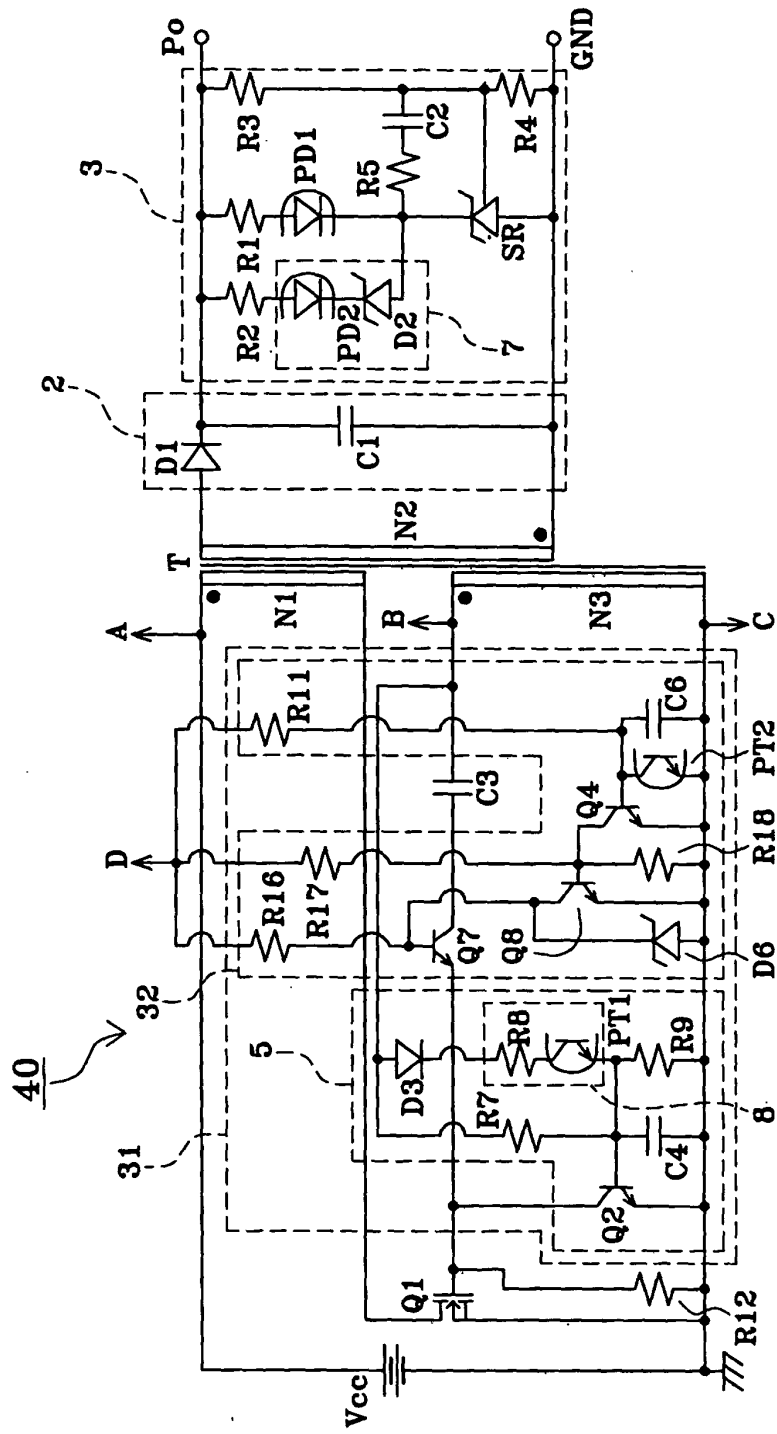




FIG. 9

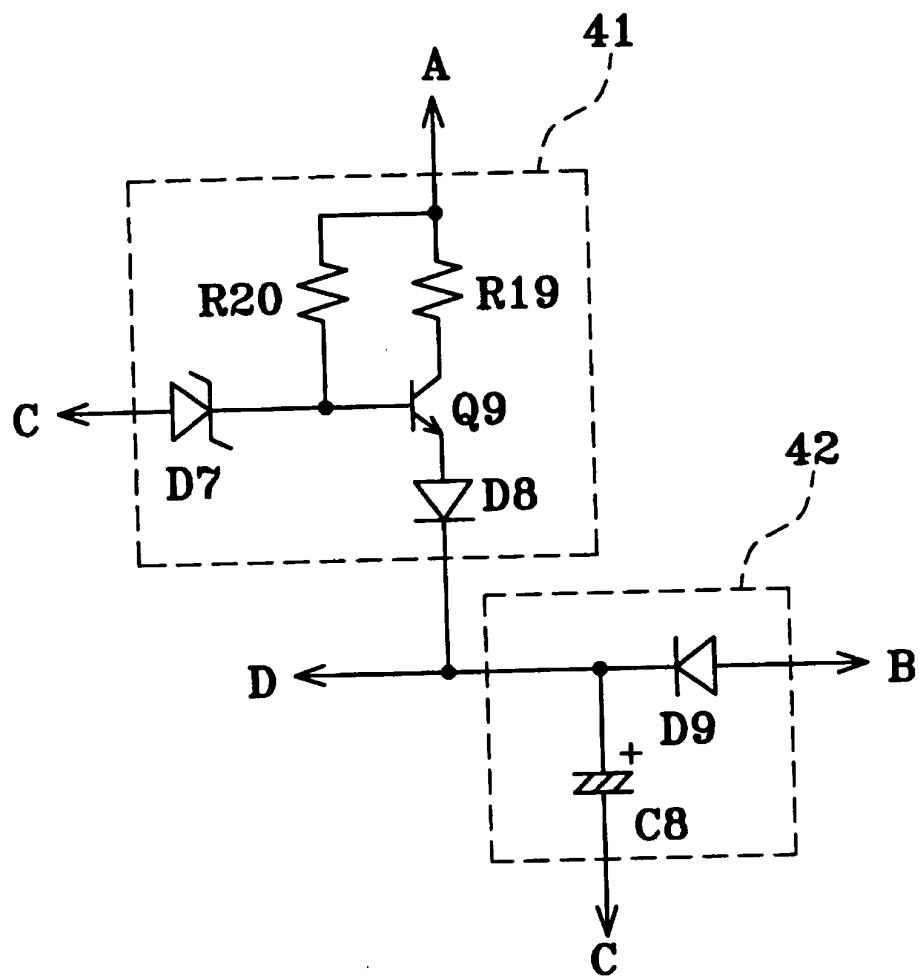


FIG. 10



FIG. 11

